WHAT IS CLAIMED IS:

1. A computer system, comprising:

a processor;

a cache associated with the processor;

system memory;

a write tracking buffer external to the processor;

wherein the write tracking buffer is operable to hold as entries the addresses of writes to system memory during the period that processor is in a low power state; and

wherein the processor is operable to invalidate the lines of cache corresponding to the entries of the write tracking buffer upon the processor exiting its low power state.

2. The computer system of claim 1, wherein the low power state of the processor comprises a non-snoopable state in which the processor is not able to monitor accesses to system memory.

3. The computer system of claim 1, wherein the write tracking buffer is maintained in a memory controller hub that is operable to track writes to system memory by bus masters operable to access system memory.

4. The computer system of claim 1, wherein the cache is an internal processor cache.

5. A method for managing the power consumption by a processor in a computer system, the computer system including system memory and the processor including an internal cache, comprising the steps of:

causing the processor to enter a low power state;

during the period that the processor is in a low power state, writing in a buffer external to the processor the addresses of modified data in system memory; and

upon the processor exiting the low power state, invalidating those lines in the cache that correspond to the memory addresses recorded in the buffer.

6. The method for managing the power consumption by a processor in a computer system of claim 5, further comprising the step of invalidating the content of the buffer.

7. The method for managing the power consumption by a processor in a computer system of claim 5, wherein the step of causing the processor to enter a low power state comprises the step of causing the processor to enter a low power state in which the processor is unable to perform the task of snooping accesses by bus masters to system memory.

8. The method for managing the power consumption by a processor in a computer system of claim 5, wherein the step of writing to the buffer the addresses of modified data in system memory comprises the step of writing to the buffer the address of each block of memory modified by a bus master of the computer system during the period that the processor is in the low power state.

9. The method for managing the power consumption by a processor in a computer system of claim 8, wherein the step of writing to the buffer the addresses of modified data in system memory comprises the step of writing the address to the buffer only if it is determined that the address has not already been written to the buffer.

10. The method for managing the power consumption by a processor in a computer system of claim 9, further comprising the step of causing the processor to exit its low power state once the buffer is full.

11. The method for managing the power consumption by a processor in a computer system of claim 5, further comprising the step of, before causing the processor to enter the low power state, writing to system memory the content of those lines of the cache that have been modified relative to the content of the corresponding locations in system memory.

12. A method for managing cache coherency in an information handling system, the information handling system including a processor with an internal cache and system memory, comprising the steps of:

performing a write back operation to write to system memory those cache lines that have been modified relative to the content of corresponding memory locations in system memory;

causing the processor to enter a low power state;

during the period that the processor is in a low power state, writing in a buffer external to the processor the addresses of data in system memory that have been modified by a bus master in the information handling system; and

upon the processor exiting the low power state for a higher power state, invalidating in the cache those cache lines corresponding to the memory addresses recorded in the buffer.

13. The method for managing cache coherency in an information handling system of claim 12, further comprising the step of clearing the buffer following the step of invalidating the cache lines corresponding to the memory addresses recorded in the buffer.

14. The method for managing cache coherency in an information handling system of claim 12, further comprising the step of, following the step of invalidating cache lines corresponding to memory addresses recorded in the buffer, writing to the invalidated cache lines the content of the corresponding memory addresses in system memory.

15. The method for managing cache coherency in an information handling system of claim 12, wherein the step of writing to the buffer comprises the step of writing to the buffer only if it is determined that the address of the modified memory location has not been previously recorded in the buffer.

16. The method for managing cache coherency in an information handling system of claim 12, further comprising the step of causing the processor to exit its low power state for a higher power state upon a determination that the buffer is full.

17. An information handling system, comprising:

a processor having an internal processor cache;

system memory;

a buffer;

a memory controller;

wherein the memory controller is operable to populate the buffer with the addresses of writes made to system memory during the period that the processor is in a low power state; and

wherein the processor, upon exiting the low power state, is operable to invalidate cache lines of the processor cache corresponding to the addresses recorded in the buffer.

18. The information handling system of claim 17, wherein the low power state is a non-snoopable state characterized by the inability of the processor to monitor writes to system memory by a bus master of the information handling system.

19. The information handling system of claim 17, wherein the memory controller is operable to cause the processor to exit its low power state when the buffer is full.

20. The information handling system of claim 17, wherein the processor is operable to perform, before entering a low power state, a write-back operation to system memory in which all modified cache lines are written to the corresponding locations in system memory.

21. A method for managing cache coherency in a computer system following the entry of a processor into a low power state, the computer system including a processor having an internal cache, system memory, and an external write tracking buffer operable to store the addresses of system memory addresses modified during the period that the processor was in the low power state, comprising the steps of:

causing the processor to exit the low power state; and

invalidating in the internal cache those cache lines corresponding to the memory addresses stored in the buffer.

22. The method for managing cache coherency in a computer system of claim 22, further comprising the step of clearing the buffer following the step of invalidating cache lines in the internal cache.

23. The method for managing cache coherency in a computer system of claim 22, further comprising the step of, following the step of invalidating cache lines corresponding to memory addresses stored in the buffer, writing to the invalidated cache lines the content of the corresponding memory addresses in system memory.